What is claimed is:

1. A method comprising:

determining a first memory buffer level for at least one memory buffer providing data to digital circuitry,

determining a second memory buffer level for a memory buffer, the second memory buffer level being set greater than the first memory buffer level,

monitoring data buffer levels in memory, and

switching digital circuitry from a first state to a second state when the monitored data buffer level is greater than the second memory buffer level, and switching the digital circuitry from a second state to a first state when the monitored data buffer level is less than the first memory buffer level.

2. The method of claim 1, further comprising switching the digital circuitry between additional states in response to changing levels of memory buffer data in at least one memory buffer.

3. The method of claim 1, wherein the first and second memory buffer level are augmented by at least one additional memory buffer level to permit greater switching control of the digital circuitry between states in response to monitored data buffer levels.

4. The method of claim 1, wherein switching the digital circuitry from the first state to the second state further comprises adjusting clock frequency of the digital circuitry.

5. The method of claim 1, wherein switching the digital circuitry from the first state to the second state further comprises adjusting voltage of the digital circuitry.

6. The method of claim 1, wherein the digital circuitry is a processor directly controlled to switch between states

7. The method of claim 1, wherein the digital circuitry is a processor controlled to switch between states in response to interactions with a power management controller.

8. An article comprising a computer-readable medium which stores computer-executable instructions, the instructions defined to cause a computer to:

determine a first memory buffer level for at least one memory buffer providing data to digital circuitry,

determine a second memory buffer level for a memory buffer, the second memory buffer level being set greater than the first memory buffer level,

monitor data buffer levels in memory, and

switch digital circuitry from a first state to a second state when the monitored data buffer level is greater than the second memory buffer level, and switch the digital circuitry from a second state to a first state when the monitored data buffer level is less than the first memory buffer level.

9. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to switch the digital circuitry between additional states in response to changing levels of memory buffer data in at least one memory buffer.

10. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to provide augmentation of the first and second memory buffer levels by at least one additional memory buffer level to permit greater switching control of the digital circuitry between states in response to monitored data buffer levels.

11. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to switch the digital circuitry from the first state to the second state by adjusting clock frequency of the digital circuitry.

12. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to switch the digital circuitry from the first state to the second state by adjusting voltage of the digital circuitry.

13. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a processor in the digital circuitry of the computer to directly control the switch between states.

14. The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a processor in the digital circuitry of the computer to be controlled to switch between states in response to interactions with a power management controller.

15. A power reduction system comprising:

a memory buffer monitoring unit to determine a first and second memory buffer level for at least one memory buffer providing data to digital circuitry, with the second memory buffer level being set greater than the first memory buffer level, and

a switching unit to adjust digital circuitry state, moving from a first state to a second state when monitored data buffer level in the memory buffer monitoring unit is greater than the second memory buffer level, and moving from a second

state to a first state when monitored data buffer level is less than the first memory buffer level.

16. The system of claim 15, further comprising switching the digital circuitry between additional states in response to changing levels of memory buffer data in at least one memory buffer.

17. The system of claim 15, wherein the first and second memory buffer level in the memory buffer monitoring unit are augmented by at least one additional memory buffer level to permit greater switching control of the digital circuitry between states in response to monitored data buffer levels.

18. The system of claim 15, wherein the digital circuitry controlled by the switching unit can be adjusted from the first state to the second state by the switching unit changing clock frequency of the digital circuitry.

19. The system of claim 15, wherein the digital circuitry controlled by the switching unit can be adjusted from the first state to the second state by the switching unit changing voltage of the digital circuitry.

20. The system of claim 15, wherein the digital circuitry controlled by the switching unit is a processor directly controlled to switch between states

21. The system of claim 15, wherein the digital circuitry controlled by the switching unit is a processor controlled to switch between states in response to interactions with a power management controller.